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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/697,751
Filing Date: October 30, 2003
Appellant: Rhee et al.

William E. Lewis
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 02, 2006 appealing from the Office action dated October 28, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US 6,122,336	Anderson	09-2000
US 6,133,773	Garlepp et al.	10-2000

US 6,295,328 Kim et al. 09-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6 and 9-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (U.S. Patent No. 6,122,336).

With respect to claims 1 and 9, Anderson discloses, in Figs. 4-5, a voltage-controlled delay line and its corresponding method comprising a delay element [404, 406, 408, 410]; and a phase interpolation circuit [412, 414] coupled to the delay element, wherein the delay element and the phase interpolation circuit are operative to (i) obtain an input signal and a complement of the input signal; and (ii) use the input signal [$A\phi_0$] and the complement of the input signal [$A\phi_4$] to perform a phase interpolation process so as to realize a complete delay timing range with respect to the input signal.

With respect to claims 2 and 10, Anderson discloses, in Figs. 4-5, that the phase interpolation process is a second-order phase interpolation process *(with first order performed by phase interpolators 412 and second order performed by phase interpolators 414)*.

With respect to claims 3 and 11, Anderson discloses, in Figs. 4-5, that the delay tuning range is equivalent to 180 degrees of a period of the input signal (*according to inputs* $A\phi_0$ and $A\phi_4$, see Fig. 5).

With respect to claims 4 and 12, Anderson discloses, that the delay tuning range is guaranteed over a process variation.

With respect to claims 5 and 13, Anderson discloses, that the delay timing range is guaranteed over a temperature variation.

With respect to claims 6 and 14, Anderson discloses, in Fig. 4, that the complement of the input signal [$A\phi_4$] is used to generate an absolute 180-degree phase reference *(inverted)*.

3. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Garlepp et al. (U.S. Patent No. 6,133,773).

With respect to claim 15, Garlepp et al. discloses, in Figs. 6 and 7, an apparatus for delaying an input signal comprising a memory [650]; and at least one processor coupled to the memory [650] and operative to (i) obtain an input signal [750] and a complement [760] of the input signal; and (ii) use the input signal [750] and the complement of the input signal [760] to perform a phase interpolation process [740] so as to realize a complete delay tuning range with respect to the input signal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (U.S. Patent No. 6,122,336) in view of Kim et al. (U.S. Patent No. 6,295,328).

With respect to claim 7, Anderson discloses, in Fig. 3 and 4, a delay-locked loop circuit comprising a voltage-controlled delay line comprising: (i) a delay element [404, 406, 408, 410], and (ii) a phase interpolation circuit [412, 414] coupled to the delay element; wherein the delay element and the phase interpolation circuit [412, 414] are operative to obtain an input signal and a complement of the input signal; and use the input signal [$A\phi_0$] and the complement [$A\phi_4$] of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal;

Anderson fails to disclose a phase detector being coupled to the voltage-controlled delay line for generating an error signal for adjusting a phase shift associated with the voltage-controlled delay line.

Kim et al. discloses, Fig. 4, a delay locked loop having a phase detector [30] coupled to a voltage-controlled delay line [32] for generating an error signal *(output of 30)* for adjusting a phase shift associated with the voltage-controlled delay line.

To configure the circuit of Anderson et al. with a phase detector as taught by Kim et al. to provide a clock generator with simplified construction and high operational safety would have been obvious to one of ordinary skill in the art at the time of the invention since Kim et al. teaches that such configuration would facilitate design simplicity and safety enhancement *(see Kim et al., col. 3, lines 26-27).*

With respect to claim 8, Anderson discloses, in Fig. 3 and 4, a clock and data recovery circuit comprising a) a clock recovery circuit [300, 308]; b) a voltage-controlled delay line comprising: (i) a delay element [404, 406, 408, 410], and (ii) a phase interpolation circuit [412, 414] coupled to the delay element; wherein the delay element and the phase interpolation circuit [412, 414] are operative to obtain an input signal and a complement of the input signal; and use the input signal [$A\phi_0$] and the complement [$A\phi_4$] of the input signal to perform a phase interpolation process so as to realize a complete delay tuning range with respect to the input signal.

Anderson fails to disclose a data recovery circuit coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line.

Kim et al. discloses, Fig. 4, a data recovery circuit [33, 34, 35] being coupled to the voltage-controlled delay line for recovering data in accordance with a clock signal received from the voltage-controlled delay line.

To configure the circuit of Anderson et al. with a data recovery circuit as taught by Kim et al. to provide a clock generator with simplified construction and increased operational safety would have been obvious to one of ordinary skill in the art at the time of the invention since Kim et al. teaches that such configuration would facilitate design simplicity and safety enhancement *(see Kim et al., col. 3, lines 26-27).*

(10) Response to Arguments

With respect to claim 1, in the paragraph linking pages 5-6, Appellant expresses the point of traversal by stating "*Anderson does not disclose use of the input signal and the complement of*

the input signal to perform a phase interpolation process ...these signals are merely clock phases generated by the ring oscillators and sent to the phase interpolation unit.". Examiner disagrees. First, as clearly shown in Fig. 4 of Anderson, [$A\phi_0$] and [$A\phi_4$] are the input signal and the complement of the input signal inputted to the phase interpolators, and second, there is no express requirement in the claims that the input signal and complement of the input signal be non-clock signal or of a particular type of signal.

Still with respect to claim 1, in the second paragraph of page 6, Appellant provides arguments that *"Anderson clearly does not provide a complete delay tuning range with respect to the input signal ... a complete delay tuning range with respect to the input signal is a tuning range of 180 degrees"*. Anderson discloses, in Figs. 4-5, input signal [$A\phi_0$] and complement of the input signal [$A\phi_4$] with 180 degree phase in reverse, which provides a complete tuning range of 180 degrees via [412,414] the process of delaying and interpolating. Thus, Anderson, indeed, does provide a complete delay tuning range with respect to the input signal of 180 degrees *(As defined in the specification, page 1, lines 15-23, a complete tuning range with respect to the input signal is a tuning range of 180 degrees).*

With respect to Appellant's argument at page 7, in the first paragraph, regarding claims 2 and 10, stating that Anderson does not seem to disclose a second-order phase interpolation process. Examiner disagrees. Anderson's Fig. 4 discloses a second-order phase interpolation process with first order performed by phase interpolators 412 and second order performed by phase interpolators 414.

With respect to Appellant's argument at page 7, in the second paragraph, regarding claims 3 and 11, stating that Anderson does not disclose that the delay tuning range is equivalent

to 180 degrees of a period of input signal. As explained above with respect to claim 1, Anderson discloses, in Figs. 4-5, input signal [$A\phi_0$] and complement of the input signal [$A\phi_4$] with 180 degree phase in reverse, which provides a complete tuning range of 180 degrees via [412,414] the process of delaying and interpolating. Thus, Anderson, indeed, does provide a complete delay tuning range with respect to the input signal of 180 degrees *(As defined in the specification, page 1, lines 15-23, a complete tuning range with respect to the input signal is a tuning range of 180 degrees).*

In response to Appellant's argument at page 7, in the third and fourth paragraphs, with respect to claims 4-5 and 11-12, stating that Anderson appears to disclose no such features as the delay tuning range is guaranteed over a process variation or temperature variation, it is noted that, in a broad interpretation, any device that is operable is guaranteed in some range of variations, whether temperature variation or process variation, since no system is perfect enough as to not to take into consideration some level of tolerances for variations. Additionally, there is no express level or range of variations in temperature or process defined by the Appellant. As such, Examiner contends that Anderson's circuit is guaranteed over process variation and temperature variation.

Similar point of traversal referencing Anderson does not disclose that the delay tuning range is equivalent to 180 degrees of a period of input signal has been addressed regarding claims 6 and 14 at page 7, in the fifth paragraph, Appellant is suggested to refer to Examiner's response regarding claim 1.

With respect to claim 15, in the paragraph linking pages 7-8, Appellant expresses the point of traversal by stating "*Garlepp does not disclose using the input signal and the*

complement of the input signal to perform a phase interpolation process to realize a complete delay tuning range with respect to the input signal.". As clearly shown in Garlepp's Fig. 7, the input signal CLK 750 and the complement of the input signal CLK\ 760 (which has a phase difference of 180 degree with respect to the input signal) being coupled to the phase interpolator 740 and the delay circuit 685 to provide a complete delay tuning range with respect to the input signal *(As defined in the specification, page 1, lines 15-23, a complete tuning range with respect to the input signal is a tuning range of 180 degrees).*

Similar point of traversal referencing "*Anderson does not disclose using the input signal and the complement of the input signal to perform a phase interpolation process to realize a complete delay tuning range with respect to the input signal.*" has been addressed regarding claims 7 and 8 at page 8, in the last paragraph. Appellant also concludes that the Anderson/Kim combination is deficient. Appellant is suggested to refer to Examiner's response regarding claim 1, and Examiner contends that the combination stated in the rejection provides the claimed limitations.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

The references to Anderson, Garlepp et al. and Kim et al. disclose a circuit that meets all limitations of the appealed claims.

For the above reasons, it is believed that the rejections should be sustained.

In addition, it is noted that under MPEP section 1205.03(A):

If the evidence appendix and related proceedings appendix are missing, but the record is clear that there is no evidence submitted and no related proceedings listed in the related appeals and interferences section, the examiner may accept the brief and state in the examiner's answer that it is assumed that the appellant meant to include both appendixes with a statement of "NONE".

As such, it is assumed by the examiner that it was appellant's intent to include both appendixes with a statement of "NONE".

Respectfully submitted,

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Conferees:

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